Statistical Approach to Robust Design of Control Schemes for Series or Parallel Connected Power Devices

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Abstract

High power, high speed operation of circuits requires that devices such as IGBTs and MOSFETs be connected in series and/or parallel. Such systems are being increasingly used in high power drives, traction, active power filters and other high power industrial applications. But no matter how perfect the design and fabrication may be, no two devices can be identical, resulting in some level of incompatibility in such systems. Therefore, there is a reduction in the overall reliability unless, care is taken to optimize the parameters of their control schemes which govern the operation of such systems. This paper reports a reliability enhancement scheme for such systems. Example of series connected IGBTs using a current feedback active gate control scheme has been considered in conjunction with the Taguchi method for this purpose. The complete strategy and calculations involved are presented, as are the experimental results to validate theoretical predictions. Results show a significant improvement in performance when the control scheme parameters are optimized using the Taguchi method. A similar approach may be followed for parallel connected devices (e.g. MOSFETs connected in parallel).

Introduction

Manufacturing very high power devices, having high switching speed capabilities has been facing technical constraints [1]. This fact, coupled with the growing popularity of insulated gate controlled devices has made the use of series/parallel connected IGBTs and MOSFETs indispensable in high power electronic applications (e.g. electric drives, traction, active power filters etc.) which require high power, fast switching devices with very high voltage or current capabilities. Over the years, several authors have reported work on series connected IGBTs [2-11], series connected MOSFETs [12], series/parallel connected IGBTs [13], parallel connected MOSFETs [14, 15] and parallel MOSFETs and IGBTs [16, 17].

The main challenge with series/parallel connection of IGBTs/MOSFETs is to ensure an equal voltage/current sharing between series/parallel connected devices, especially during transients. Imbalance in current/voltage sharing leads to unequal switching energies associated with the devices which, in turn, leads to thermal asymmetry and failure [15]. Fig. 1 shows the burnt out dices of series connected IGBTs subjected to overvoltage. This is highly undesirable since such systems are usually very expensive. Thus, there is a need for schemes which can ensure that this does not happen. Further, for a given scheme, there is a need to study the limits to which the system operation can be stretched without compromising with its performance.

The general approach for designing a system with enhanced power capabilities is highlighted in Fig. 2. Several schemes have been proposed for effective connection of these devices [1-7, 9, 11, 12, 14-17]. Each scheme has its own set of operating limits, advantages and disadvantages. Therefore, it is necessary to go for a control scheme which is most appropriate for a given application. An improper selection of a control technique may result in reduced reliability, high cost and low performance. Further, just a proper selection of a control scheme may not be adequate, unless the control parameters are optimized for the desired performance and the operating limits are known.

(a)

(b)

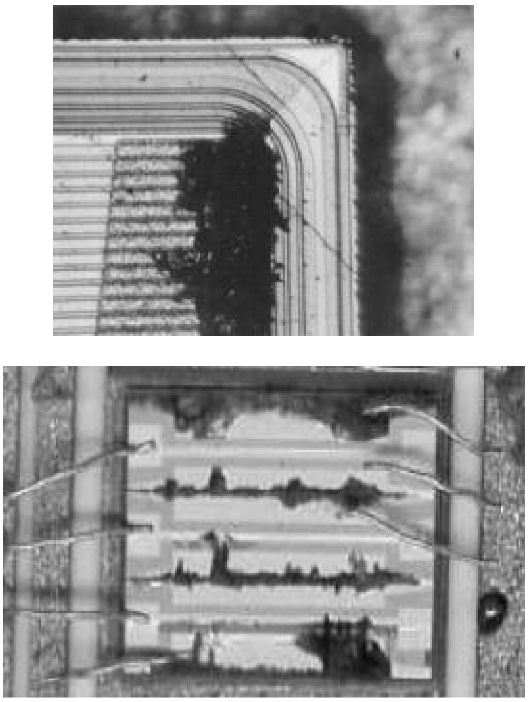

Fig. 1: Burnt-out dices of series-connected IGBTs subjected to unequal voltage sharing leading to over-voltage failure. [Courtesy: Microsemi Power Products Group]

From the preceeding paragraph it follows that while selecting a control scheme for a given application, there is a need for the following:

– a procedure to determine the optimum operating limits for the given scheme;
– a procedure for fine tuning the given scheme to make it more robust under changing operating conditions.

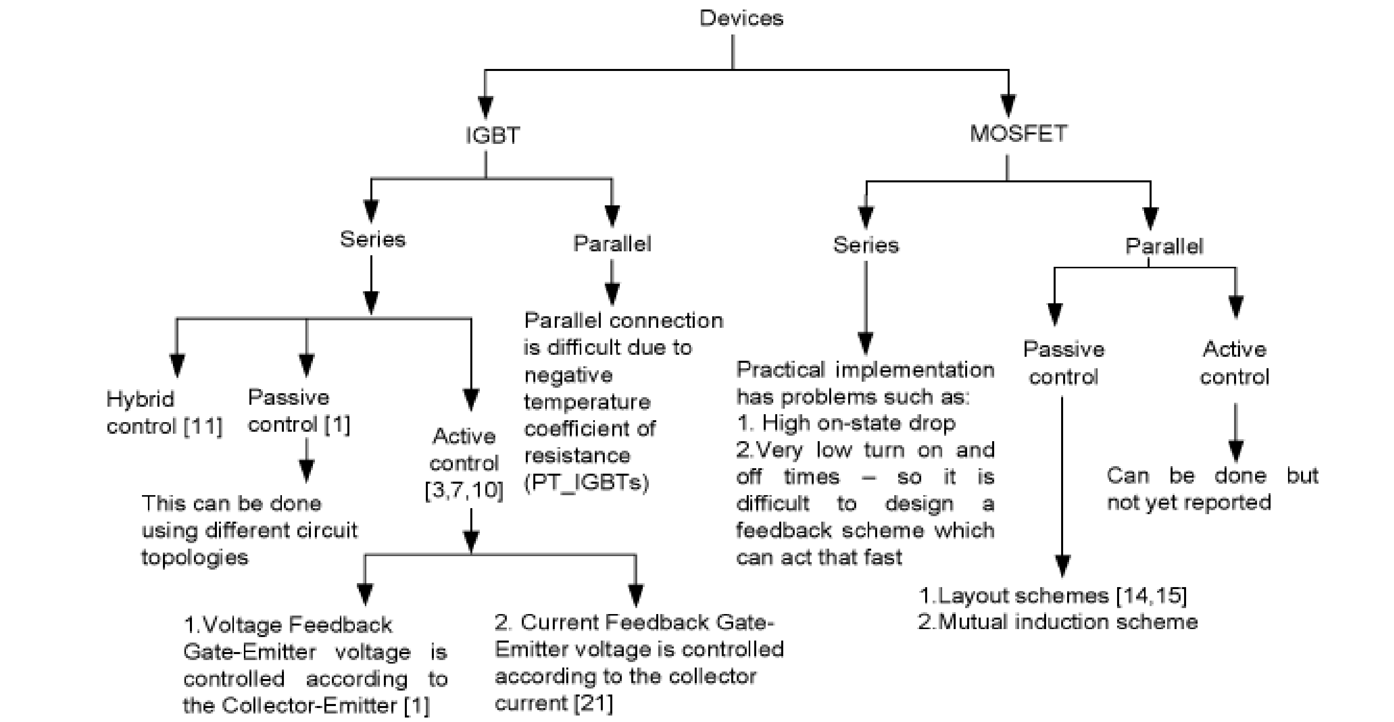

Fig. 2: Categorization of the available techniques for series-parallel connection of power devices

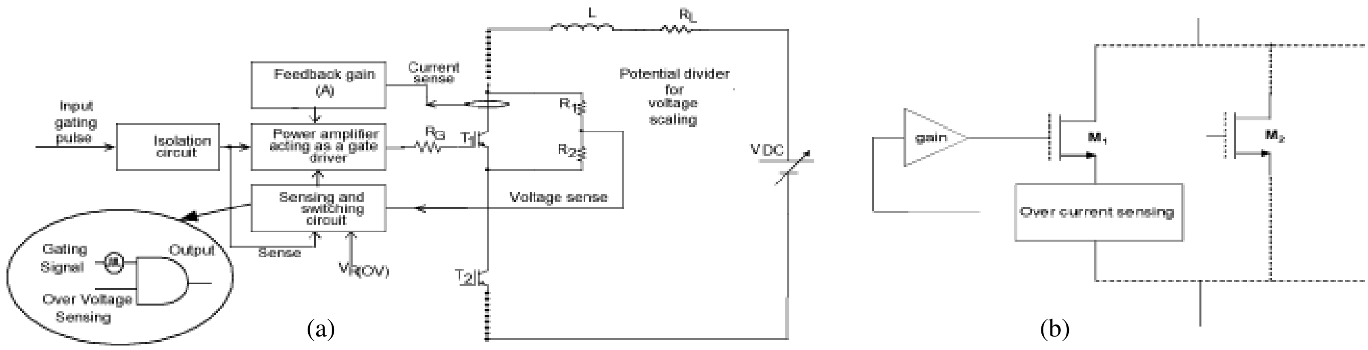

Fig. 3: (a) Positive current feed back system [19] for series connected IGBTs (similar circuits are used across all the devices in series) used in a class-A chopper circuit. L is stray inductance and R_L is the load. This circuit was simulated in PSPICE to achieve Taguchi method based optimization; (b) Block diagram representation of parallel connected MOSFETs using active gate control scheme.

Taguchi method has been extensively used to increase the robustness of several systems [18–20] under changing operating conditions (e.g. input levels, currents, voltages, frequency, temperature, ageing etc.). This method follows a statistical approach to map the system response to variations in control factors under the influence of changes in other control factors and noise levels. Thus, this approach is more relevant to an actual, practical system. The work presented in this paper uses Taguchi approach.
The objectives of this paper are to:

– propose a procedure for setting proper, optimum operating limits for control schemes corresponding to series or parallel connected power devices;
– define a procedure to make a given control scheme more robust;
– present a case study for an example control scheme.

The example control scheme considered in this work is the "current feedback active gate control technique" applicable to series connected IGBTs as shown in Fig. 3(a). Similar approach can be extended to other schemes used for series/parallel connected IGBTs/MOSFETs. Fig. 3(b) shows a parallel connected MOSFETs scheme.

Current feedback active gate control of series connected IGBTs

Active Gate Control (AGC) [1, 2, 3, 6, 7, 9, 17, 21] provides an excellent solution for the problems associated with series connected IGBTs. AGC involves the operation of IGBTs in active region to control the over-voltage, whenever required. AGC may either use the device voltage feedback or the device current feedback. In the voltage feedback method [9], over-voltage across the device is sensed and the gate voltage is controlled according to the level of over voltage, with an appropriate gain. Different methods of voltage feedback use different approaches to determine the value of the feedback gain. But the voltage feedback system suffers from the following drawbacks:

– it affects the reliability of the series connected devices [9] due to rapid rate of rise and fall of voltages across each IGBT (both across the gate-emitter and collector-emitter);
– operation over wide range of load currents is very difficult due to the highly nonlinear characteristics of the IGBTs;
– the control system design involves complex calculations.

Current feedback method [21] overcomes the above mentioned drawbacks. In this scheme, the voltage across the IGBT is controlled by feeding back a voltage into the gate which is proportional to the current through the device. The method employs a current feedback network which acts only in case of an overvoltage across the device (IGBT) under consideration.

Fig. 4 shows the I_C (collector current) versus V_{GE} (gate-emitter voltage) curve for a constant value of V_{CE} (collector-emitter voltage) and constant temperature. The advantage of positive current feedback technique is that it is not susceptible to changes in temperature [21]. Once the feedback comes into action, the gate voltage is controlled according to the current through the device (I_C). The current feedback network works as per the following equation:

$$V_{GE} = V_{GT} + (A) \times (I_C) + P \text{ (for } V_{CE} > V_{R(OV)}\text{)} \quad (1)$$

where the difference between the gate threshold voltage of the device and the X-intercept of the curve used for feedback is denoted by *P*, while the feedback gain is denoted by *A*. Thus, as the gate voltage increases, the collector emitter voltage reduces, thereby protecting the system. But any reduction in the collector emitter voltage results in an increase in the device current. Hence, the system acts as a positive feedback system. In order to avoid any instability arising due to this positive feedback, a switching network is used which prevents the positive current feedback system from going into instability (in physical sense, switching network does not allow the IGBT to go into complete conduction) which may result due to the difference between actual curve and the curve (dotted) used for practical feedback purposes as shown in Fig. 4.

Practically, there exists a time lag between the occurrence of overvoltage and the time after which the feedback system comes into complete action. Hence, there occurs an Over Voltage Spike (OVS). Taguchi method can be used to design the system parameters so as to reduce the OVS. OVS is the difference between the actual maximum voltage appearing across the device and threshold limit setting used in the control system. The value of OVS is dependent on many parameters such as P, A, operating current etc. (refer to Fig. 4). Any attempt to decrease this over voltage by adjusting the parameters would result in an increased Under-Voltage Level (UVL) – the amount by which the voltage falls below the threshold limit setting. UVL is a result of the delay in the switching network's action after the device voltage falls below the threshold limit as a result of feedback.

The increase in UVL across one of the devices results in an increase of voltage levels across other IGBTs in series which are about to turn off completely, activating their respective feedback circuits and taking them into conduction one by one in a chain like manner. This may result in an unstable operation. Thus, while the risk of over-voltage results in derating of the device, under voltage causes instability in the operation of the series connected IGBTs.

Importance of fine tuning and optimization

In the current feed back system, a decrease in OVS may be achieved by any of the following:

– by increasing the feedback gain (A);
– by increasing the difference between the gate threshold voltage

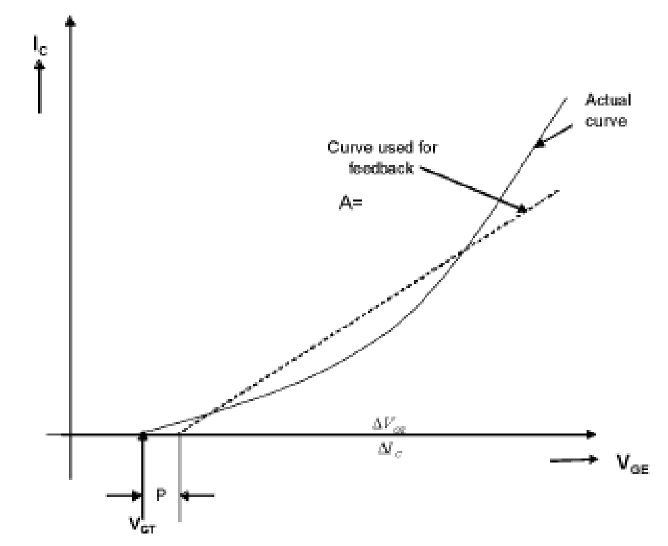

Fig. 4: I_C versus V_{GE} curve of an IGBT for a constant V_{CE}

of the device and the X-intercept of the curve used for feedback (P) [See Fig. 4];
– by reducing the gate resistance, R_G.

One might be tempted to change the values of A, P and R_G arbitrarily, such that OVS vanishes completely. But this will result in a corresponding increase in UVL, which in turn affects the stability of the system. This conflicting constraint implies there exists a trade-off between OVS and UVL. A good compromise would be to keep the value of 'OVS + UVL' as low as possible by optimizing the values of A, P and R_G, rather than trying to optimize OVS and UVL individually. This is where a statistical optimization approach, such as the Taguchi method, is needed.

Robust design of the current feedback system

Design of experiment (DOE) using Taguchi approach is a popular tool among the design engineers. Standard procedures have been formulated for each of the DOE application steps [18–20]. The main objective of Taguchi experiment design technique is to minimize the variation in the output function leading to a robust design. DOE requires the identification of the following items.

Control factors

The control factors can be:

– design parameters that directly influence system performance;
– controllable input(s) to the system.

The control factors in the design of the given current feedback system are the feedback gain (A), Gate resistance (R_G) and P [See Fig. 3]. The DC link voltage (V_{DC}) is the input (control) factor.

Noise factors

These are uncontrollable, unpredictable factors enforced by the operating environment. A given noise factor is 'noise' only if it influences one or more performance parameters. In view of this, the effects of operating environmental conditions (e.g. temperature) on the system performance should be clearly known. For the given current feedback system, the following noise factors are considered:

Table 1: List of the factors used along with their levels

Factor	Symbol	Type	Number of levels	Value of each level
Feedback gain (A)	A	Control Factor	3	$A_1 = 0.250$, $A_2 = 0.270$, $A_3 = 0.290$.
Gate resistance (R_G)	B	Control Factor	3	$B_1 = 50\ \Omega$, $B_2 = 100\ \Omega$, $B_3 = 150\ \Omega$
[Gate threshold Voltage(V_{GT}) – X intercept of the actual line used for the feedback] = P	C	Control Factor	3	$C_1 = 0.3$ V, $C_2 = 0.4$ V, $C_3 = 0.5$ V.
Temperature	N	Noise	3	$N_1 = 10$ °C, $N_2 = 40$ °C, $N_3 = 60$ °C.
Max. on-state current	I_C	Noise	3	$I_{C1} = 10$ A, $I_{C2} = 25$ A, $I_{C3} = 40$ A.
DC link Voltage	V_{DC}	Input	3	$V_1 = 250$ V, $V_2 = 400$ V, $V_3 = 550$ V.

– temperature, which depends on the environmental conditions;
– the maximum operating current (I_{Cmax}), which is application dependent.

Factor levels

It is important to consider appropriate levels (values) of the control and noise factors for a given application. To do this, it is necessary to know the following:

– the range of values which these factors can assume within the application's legitimate operating limits;
– once the range is known, it should be applied in proper steps. Both accuracy and feasibility should be kept in mind while choosing the step size.

For the system considered in this work, the factor levels considered are shown in Table 1.

Interaction between factors

Another important issue is to determine the interaction levels between the different control and noise factors. In this context, it is desirable to know:

– Which factors are most likely to interact?
– How many of these interactions are feasible to be considered for analysis?

The complexity of the analysis depends on the number of factors and their interactions considered, which in turn depends on factors such as how many experiments is it feasible to run, how much time is available for the same and what are the costs involved. Accuracy is another important factor. In this work, an L_{18} orthogonal array [refer to Table 2] has been used corresponding to eighteen combinations of three control factors, with three levels each. Depending on the number of variables involved, and practical reasons, the number of experiments is minimized by discarding the redundant cases. In our work, the number of variables is 3, with each variable associated with 3 levels. Hence, the total number of combinations is 27 and so many experiments should ideally be conducted. But it is sufficient to consider only 18 combinations (denoted by L18[19]) for the experiments as the rest can be shown to be redundant and are not really required. Three levels of each noise factor are also considered and the number of noise levels turns out to be nine [= ${}^3C_1 \times {}^3C_1$]. Similarly, three levels (250 V, 400 V, 550 V) of input DC link voltage (input factor) are considered for the analysis.

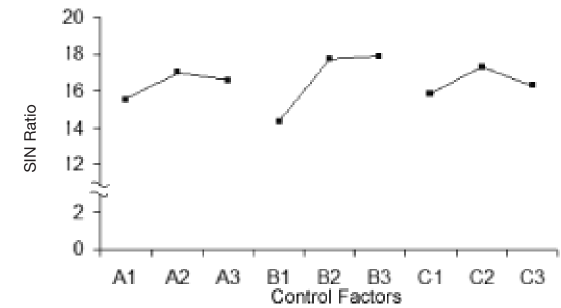

Fig. 5: S/N ratios computed and plotted for different control factors

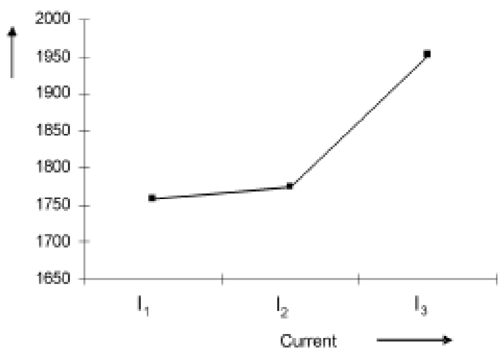

Fig. 6: IGBT collector current versus variance of the output function

Output function

The performance of a system is measured in terms of the parameters of interest. These parameters are combined (mixed) in a suitable manner to form an output function. The objective of Taguchi technique is to minimize the variation in this function. In our current feedback system, the output function is taken to be "OVS + UVL" which incorporates both stability and over voltage limit. This has already been described above.

Table 2: L_{18} along with the S/N ratios calculated for each combination of control factor levels

S.No.	Control factors			Noise level	Output(v)= (O.V-U.V) for inputs =			L	S/N ratio
	A	R_G	P		250 V	400 V	550 V		
1	1	1	1	N_1, I_1	107	101	98	100.875	13.01
				N_1, I_2	148	159	167	160.375	
				N_1, I_3	171	178	181	177.916667	
				N_2, I_1	109	106	111	108.916667	
				N_2, I_2	148	161	161	158.291667	
				N_2, I_3	167	183	190	182.875	
				N_3, I_1	107	112	119	114.166667	
				N_3, I_2	148	157	163	157.875	
				N_3, I_3	173	187	198	189.125	
2	1	1	2						9.05
3	1	2	3						13.80
4	1	2	1						17.22
5	1	3	2						19.73
6	1	3	3						17.55
7	2	1	1						11.59
8	2	1	2						18.19
9	2	2	3						18.09
10	2	2	1						18.55
11	2	3	2						19.38
12	2	3	3						17.18
13	3	1	1						11.21
14	3	1	2						17.88
15	3	2	3						18.34
16	3	2	1						17.67
17	3	3	2						18.99
18	3	3	3						17.36

Analytical and experimental results

Table 2 shows the array of 18 combinations used along with their S/N ratios obtained using repeated PSPICE simulations. The circuit shown in Fig. 3(a) was simulated with various combinations of control and other parameters (shown in Table-2). The *S/N* ratio for "Nominal-the-best" case is defined by [19]:

$$S/N = 10\log\left(\frac{\mu^2}{\sigma^2}\right) \tag{2}$$

where μ is the mean and σ^2 is the variance of the proportional function L, given by the following expression:

$$L = \frac{\Sigma(output\ function) \times (input\ V_{DC})}{\Sigma(input\, V_{DC})} \tag{3}$$

Three values each of the control factors A, P and R_G are considered. Fig. 5 shows the variation of *S/N* ratio as a function of various control factors. Only one level of a control factor is considered at a time, while the levels of all other control and noise factors are varied in all possible combinations present in the orthogonal array. From Fig. 5 it is clear that the combination of A_2, B_3 and C_2 gives the best results, since they correspond to maximum *S/N* ratios.

Fig. 6 shows the change in the variance of L with respect to the operating current. An abrupt increase in the variance, as the current changes from I_2 (25 A) to I_3 (40 A), is noteworthy since it suggests that the proposed feedback circuit would work better for the current range 0–25 A, giving higher *S/N* ratios. For still better performance, the circuit may be further optimized in the current range 0 – 25A. Fig 7 shows the Gate-emitter and collector-emitter voltages corresponding to the devices S_1 and S_2 when no feedback is used. Fig. 8 shows the Gate-emitter and collector-emitter voltages corresponding to the devices S_1 and S_2 when the proposed feedback network is used.

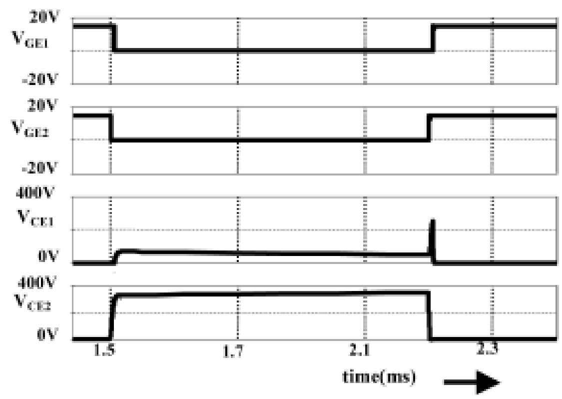

Fig. 7 Gate-emitter and collector-emitter voltages corresponding to the devices S_1 and S_2 when no feedback is used. Delay between the gating pulses = 5 μs; ON-state operating current ≈ 25A.

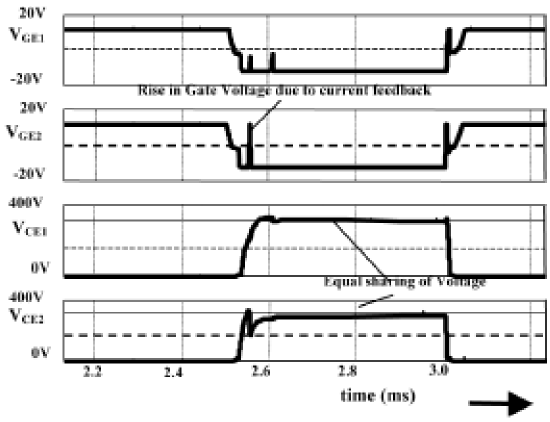

Fig. 8: Gate-emitter and collector-emitter voltages corresponding to the devices S_1 and S_2 when the proposed feedback network is used. Delay between the gating pulses = 5 μs; ON-state operating current ≈ 25A.

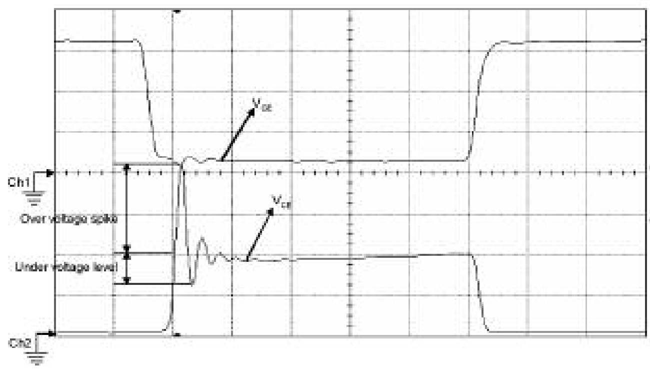

Fig. 9: Experimental waveforms of gate-emitter and collector-emitter voltages of the top IGBT,with current feedback without optimization. [x-axis: 9.02 μs/div, y-axis: channel 1 = 5 V/ div, channel 2 = 50 V/div, frequency of operation = 10 kHz, DC link voltage = 200 V, on-state current = 2.2 A].

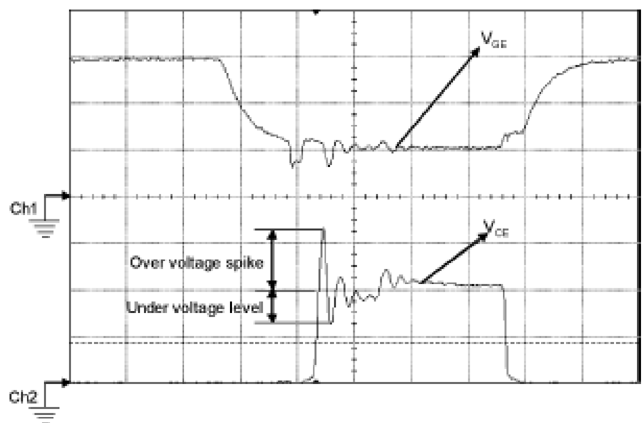

Fig. 10 Experimental waveforms of gate-emitter and collector-emitter voltages of the top IGBT, with current feedback using the robust (optimized) design [x-axis: 9.02 μs/div, y-axis: channel 1 = 5 V/div, channel 2 = 50 V/div, frequency of operation = 10 kHz, DC link voltage = 200 V, on-state current = 2.2 A]. Optimized control factor combination of A_2, B_3, C_2 has been used.

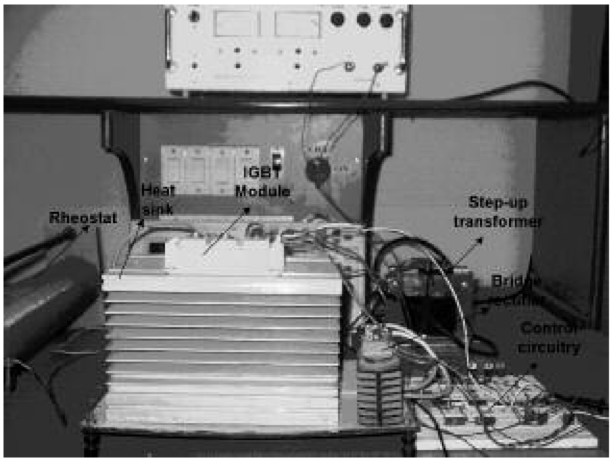

Fig. 11: Photograph showing the experimental set-up used in the experiments

The prototype of a buck (class A chopper) circuit [Fig. 3] was built in the laboratory. Two IGBTs (Siemen's BSM100GB120DN) were connected in series to realize a high voltage switching device. Even though the device can withstand up to 1200 V, due to limited laboratory facilities and other practical constraints, the experimental values were restricted to lower voltages. Two sets of experiments were conducted - one with the optimum values corresponding to A_2, B_3 and C_2 and the other with arbitrary, un-optimized values. Fig. 9 shows the experimental waveforms of the top device voltage and the corresponding gate-emitter voltage without optimum values. Fig.10 shows the corresponding waveforms with optimized control parameters. Agilent's Infiniium oscilloscope (model 54810A) was used in the experiments. A photograph of the experimental set-up used is shown in Fig. 11. The reduction in the value of the output function "OVS + UVL" in case of optimized values is clearly visible. The variance with respect to the mean value of "OVS + UVL" remains minimum over a wide range of operating conditions, when optimized control factor values are used.

Conclusions

Importance of a statistical optimization technique has been demonstrated for series or parallel connected power devices. The need for a robust design of such systems has been emphasized. Further, the importance of setting appropriate operating limits for a given control scheme has been highlighted. The statistical approach, such as the Taguchi method, not only helps in realizing a robust design but also determines the operating limits for a particular control system during the simulation stage itself – i.e. before actual hardware implementation. This approach enhances the life of electrical and electronic systems and is particularly useful for high power systems which are very expensive. Specific example of series connected IGBTs with active gate control using positive current feedback has been included to demonstrate the usefulness and relevance of the proposed idea. A similar approach can be used for parallel/series connected MOSFETs and other high power devices.

References

[1] Application note, APT0405, November 2004, Microsemi Corporation - http://www.microsemi.com/support/micnotes.asp

[2] C. Abbate, G. Busatto, L. Fratelli, F. Iannuzzo, B. Cascone, G. Giannini: Series connection of high power IGBT modules for trac-

tion applications. European Conference on Power Electronics and Applications, Dresden, Germany, 11-14 Sept. 2005.

[3] J. Sigg, M. Bruckmann, P. Turkes: The Series Connection of IGBTs Investigated by Experiments and Simulation", 27th Annual IEEE Power Electronics Specialists Conference, vol. 2, pp. 1760-1765, 1996.

[4] J.M. Bodson, J. B. Saada, A. Colasse A., P. Colignon, L. Delporte L., J. E. Masselus, P. Mathys, M. Osée: Study of direct series connection of IGBT for a 3 kV chopper, in Proc. 8th European Conf. Power Electronics and Applications (EPE'99), Lausanne, Switzerland, pp.1–9, Sept. 7–9, 1999.

[5] P.R Palmer, H.S. Rajamani, N. Dutton: The use of capsule IGBTs in the series connection, Eighth IEE International conference on Power Electronics and Variable Speed Drives, pp. 250-255, Sept 2000.

[6] U. Schwarzer, R.W. De Doncker, R. Sommer, G. Zaiser: Snubberless Operation of Series Connected 6.5 kV IGBTs for High-Power and High-Voltage Applications, European Conference on Power Electronics and Applications (EPE2003), Toulouse, France, 2-4 September, 2003.

[7] G. Belverde, A. Galluzzo, M. Melito, S. Musumeci, A. Raciti: Snubberless voltage sharing of series-connected insulated-gate devices by a novel gate control strategy, IEEE Transactions on Power Electronics, vol. 16, no. 1, pp. 132-141, 2001.

[8] A. Nagel, S. Bernet, T. Bruckner, P.K. Steimer, O. Apeldorn: Design of IGCT series connection for 6 kV medium voltage drives, IEE Seminar on PWM Medium Voltage Drives, pp. 2/1-2/5, 11 May 2000.

[9] P.R Palmer, A.N. Githiari: The series connection of IGBTs with active voltage sharing, IEEE Transactions on Power Electronics, vol. 12, no. 4, pp. 637-644, 1997.

[10] P.R Palmer, A.N. Githiari, R.J. Leedham: A comparison of IGBT technologies for use in the series connection, sixth IEE International conference on Power Electronics and Variable Speed Drives, Nottingham, pp. 23-25, Sept 1996.

[11] R. Withanage, W.Crooks, N.Y.A. Shammas: Novel voltage balancing technique for series connection of IGBTs, European Conference on Power Electronics and Applications, pp. 1-10, Sep. 2007.

[12] R. Guidini, D. Chatroux, Y. Guyon and D. Lafore: Semiconductor power MOSFETs devices in series, Fifth European conference on Power Electronics and Applications, vol. 2, pp. 425-430, Sept 1993.

[13] N.Y.A Shammas, R. Withanage, D. Chamund D: Review of series and parallel connection of IGBTs, IEE Proceedings on Circuits, Devices and Systems- vol. 153, Feb. pp. 34 – 39, 2006.

[14] K. Reinmuth, H. Amann: Ruggedness of Paralleled Power MOSFETs; Fifth European Conference on Power Electronics and Applications, vol. 2, pp 680 -684, 1993.

[15] T. Matsukawa, K. Shimada, M. Shioyama, J. Nomura, T. Takaku, S. Tsuji-Iio, R. Shimada: Advanced application of power-MOSFET to large capacity converter, Proceedings of the Power Conversion Conference, Osaka, pp 1170 -1175, 2002.

[16] P. Jeannin, J. L. Schanen, E. Clavel: Original cabling conditions to insure balanced current during switching transitions between paralleled semiconductors, IEEE Transactions on Industry Applications, vol. 38 , pp 181 -188, 2002.

[17] Klaus F. Hoffmann, Jens Peter Karst: High Frequency Power Switch - Improved Performance by MOSFETs and IGBTs Connected in Parallel, European Conference on Power Electronics and Applications (EPE 2005), Hamburg, Germany, 11-14 Sept. 2005.

[18] G. Taguchi: Quality engineering (Taguchi methods) for the development of electronic circuit technology, IEEE Transactions on Reliability , vol. 44, no. 2, pp. 225 -229,1995.

[19] Madhav S. Phadke: Quality Engineering using Robust Design, Prentice-Hall International, Inc., 1989.

[20] D. Hissel, P. Maussion, J. Faucher: On evaluating robustness of fuzzy logic controllers through Taguchi methodology, Proc. of the 24th Annual Conference of the IEEE Industrial Electronics Society IECON '1998, Aachen, Germany, vol. 1, pp. 17-22.

[21] D.V.M.M. Krishna and Vivek Agarwal: Active Gate Control of Series Connected IGBTs using Positive Current Feedback Technique, IEEE Transactions on Circuits and Systems – II, vol. 52, no. 5, pp. 261-265, 2005.

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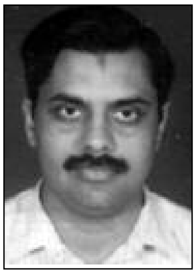

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